Remarks

Applicant respectfully requests reconsideration of this application as amended. Claims 1 and 10 have been amended. No claims have been canceled. Therefore, claims 1-29 are presented for examination.

Claims 1-29 stand rejected under 35 U.S.C. 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant submits that the term "data access primitive" is not indefinite.

In the Specification, data access primitives are defined as logic design components that may be used by a designer to specify an assembly of address and lane matching logic. See Specification at page 7, lines 4-6. The Examiner asserts that:

> Applicant variously describes said terms as: "hides the details . . . abstracts away the interdependencies" at Remarks page 12. It is not clear how said "data access primitive" hides or implies said details and interdependencies and functions.

See Office Action at page 4, paragraph 22. The Examiner also maintains that:

> It is not clear how said "data access primitive" can "model said "address matching function..." while hiding or abstracting the details and interdependencies".

See Office Action at page 4, paragraph 23.

Applicant submits that a function of a data access primitive is to imply address-matching functions, lane-matching functions, data bus connections for one or more bytes of data and auxiliary logic. See Specification at page 7, lines 6-8. However, such a function is not the definition of a data access primitive. As described above, a data access primitive is a logic design component that may be used to specify an assembly of address and lane matching logic. Therefore, applicant submits that the term "data access primitive" is not indefinite.

Further, the Examiner has interpreted the term "data access primitive" according to various definitions. Applicant has expressly denied such interpretations in previous responses. For instance, applicant has, and continues to, maintain that "data access primitive" be interpreted as described in the Specification.

Claims 1, 18 and 24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Dangelo (U.S. Patent No. 6,324,678) in view of Tabak. Applicants submit that the present claims are patentable over Dangelo in view of Tabak.

Dangelo discloses an electronic CAD system operated with a suite of software tools for enabling a designer to create and validate a structural description and physical implementation of a device from a behavior-oriented description using a high-level computer language. First, a designer specifies the desired behavior of the device in a high-level language, such as VHDL. The description includes high-level timing goals. Next, the designer iterates through simulation and design changes until the desired behavior is obtained. Next, the design is partitioned into a number of architectural blocks by exploring the "design space" of architectural choices, which can implement the design behavior. Next, in a "logic synthesis" step, a number of separate programs are used to efficiently synthesize the different architectural blocks identified in the partitioning step. Those blocks having highly regular structures or well understood functions are directed to specific synthesis tools (e.g. memory or function compilers). Those blocks with random or unstructured logic are directed to more general logic synthesis programs. The output of this step is a net list of the design. Next, in a "physical simulation" step, the gate-level design description is simulated, comparing the results with those from the initial behavioral simulation. Finally the design is input to existing software systems that control the physical implementation of the design, such as in an ASIC (Application Specific Integrated Circuit) device. See Dangelo at col. 3, ll. 35 – col. 4, ll. 28.

However, Dangelo does not disclose or suggest replacing a data access primitive with logic components that implement a first set of addressing matching function, lane

matching function and one or more bus connections for the memory-mapped device based upon the data access primitive and the first starting address.

Tabak discloses various microprocessor architectures. However, claim 1 of the present application recites replacing a data access primitive to logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for a memory-mapped device based upon the data access primitive and a first starting address.

Applicant submits that nowhere in Dangelo or Tabak is there disclosed a data access primitive as recited in claim 1. As discussed above, a data access primitive is a logic design component used to specify an assembly of address and lane matching logic. Neither Dangelo nor Tabak disclose or suggest address and lane matching logic. Tabak does disclose a processor that features cache memory mapping. Nevertheless, memory mapping is not equivalent to address and lane matching. Therefore, since neither reference discloses or suggests address and lane matching, Dangelo and Tabak cannot disclose data access primitives.

Similarly, since Dangelo and Tabak do not disclose or suggest data access primitives, the references cannot disclose or suggest replacing a data access primitive to logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for a memory-mapped device. Moreover, because neither Dangelo nor Tabak disclose or suggest replacing a data access primitive to logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for a memory-mapped device, any combination of Dangelo and Tabak would also not disclose or suggest such a feature. Accordingly, claim 1 is patentable over Dangelo in view of Tabak.

Claims 2-9 depend from claim 1 and include additional features. Thus, claims 2-9 are also patentable over Dangelo in view of Tabak.

Claim 10 recites replacing a data access primitive to logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for a memory-mapped device based upon the data access primitive and a first starting address. Thus, for the reasons described above with respect to claim 1, claim 10 is also patentable over Dangelo in view of Tabak. Because claims 11-17 depend from claim 10 and include additional limitations, claims 11-17 are also patentable over Dangelo in view of Tabak.

Claim 18 recites generating first logic components that implement an address matching function, and generating second logic components that implement lane matching function and one or more bus connections. There is no disclosure or suggestion in Dangelo or Tabak of generating logic components that implement address matching and lane matching functions, or one or more bus connections. Therefore, claim 18 is also patentable over Dangelo in view of Tabak. Since claims 19-23 depend from claim 18 and include additional limitations, claims 19-23 are also patentable over Dangelo in view of Tabak.

Claim 24 recites generating first logic components that implement an address matching function, and generating second logic components that implement lane matching function and one or more bus connections. Thus, for the reasons described above with respect to claim 18, claim 24 is also patentable over Dangelo in view of Tabak. Since claims 25-29 depend from claim 24 and include additional limitations, claims 25-29 are also patentable over Dangelo in view of Tabak.

Claims 2-17, 19-23 and 25-29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Dangelo in view of Tabak and Applicant's Admission and MPEP 2144.04 (Routine Expedient of making automatic). Applicant submits that the present claims are patentable over Dangelo and Tabak even in view of background pf the application.

Applicant's background discloses specifying the addressability and bus connections, and the tediousness of a designer to explicitly specify designing for 8-bit and 32-bit system busses. See Specification at pages 1 and 2. However, if anything, applicant's background teaches away from the claims since the claims recite generating first logic components that implement an address matching function, and generating second logic components that implement lane matching function and one or more bus connections.

As described above, neither Dangelo nor Tabak disclose or suggest address and lane matching functions. Therefore, the present claims are patentable over any combination of Dangelo, Tabak and applicant's background since none of the above disclose or suggest generating first logic components that implement an address matching function, and generating second logic components that implement lane matching function and one or more bus connections.

Applicant respectfully submits that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
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